CLAIMS:

1. An electronic data processing circuit, the circuit comprising

- a plurality of data handling units (10a-d, 16a-b) with data outputs, at least part of the data handling units having address outputs;
- a bus (14) with address lines and data lines, the data lines supporting simultaneous transfer of up to a maximum number of bits in a bus cycle;
- a bus controller (20) coupled to the data handling units and arranged to control access to the bus in successive access cycles, the bus controller (20) being arranged to cause data bits from a plurality of data words of less than said maximum number of bits, from respective ones of the data handling units (10a-d, 16a-b), to be placed in combination on the data lines in a same bus cycle, the bus controller (20) causing write addresses that the respective ones of the data handling units (10a-d, 16a-b), supply for respective ones of the plurality of data words to be placed on the address lines in a plurality of respective bus cycles.

2. An electronic data processing circuit according to Claim 1, wherein the data handling units (10a-d) support a variable word size, the bus controller (20) adapting a number of words in the plurality of data words that is placed on the data lines to the word size or word sizes supplied by the data handling units (10a-d, 16a-b).

3. An electronic data processing circuit according to Claim 1, wherein the bus controller (20) is arranged to select a distribution of which bits of the plurality of words will be placed on which of the data lines in said same cycle, dependent on an evaluation that takes account of a number of data lines that will change logic level upon placing the bits of the plurality of words on the data lines, the bus controller (20) selecting a distribution that minimizes the number of data lines that will change logic level among at least two possible distributions.

4. An electronic data processing circuit according to Claim 3, wherein the bus controller (20) selects the distributions from permutations of placements of the plurality of words on the data lines.

5. An electronic data processing circuit according to Claim 4, wherein the bus controller (20) causes the addresses that the respective ones of the data handling units supply for respective ones of the plurality of data words to be placed on the address lines in successive bus cycles, in a sequence wherein a position of the address is dependent on the position where the corresponding word is placed on the data lines.

6. An electronic data processing circuit according to Claim 1, wherein at least one of the data handling units (16a-b) is a memory unit, the bus controller being arranged to include, among said plurality of data words that is placed in combination on the data lines in a same bus cycle, a read result produced by said memory unit (16a,b) when available.

7. An electronic data processing circuit according to Claim 6, wherein the control circuit (20) is arranged to adjust a number of bus cycles in the plurality of respective bus cycles in which addresses are placed on the address lines for respective ones of the plurality of data words, said number being adjusted dependent on a further number of read results that is included in the plurality of data words.

8. An electronic data processing circuit according to Claim 1, comprising a data receiving circuit (16a,b) coupled to the bus (14), the data receiving circuit (16a,b) being arranged to handle multi bus cycle data transfers via the bus (14) using a single start address supplied via the address lines, the bus controller (20) being arranged to place the addresses that the respective ones of the data handling units (10a-d) supply for respective ones of the plurality of data words on the address lines in bus cycles corresponding to a multi bus cycle data transfer wherein the multi bus cycle data transfer involves no address transfer.

9. An electronic data processing circuit, the circuit comprising

- a plurality of data handling units (10a-d, 16a,b) with data outputs, at least part of the data handling units (10a-d) having and address outputs for writing words of data;
- a bus (14) with address lines and data lines;

- a bus controller (20) coupled to the data handling units and arranged to control access to the bus (14) in successive access cycles, the bus controller being arranged to select a distribution of when and/or where words from the data handling units will be placed on the data lines of the bus (14), dependent on an evaluation that takes account of a number of data lines that will change logic level upon placing the words on the data lines, the bus controller (20) selecting a distribution that minimizes the number of data lines that will change logic level among at least two possible distributions.

10. An electronic data processing circuit according to Claim 9, wherein the bus controller (20) is arranged to select the distribution of a plurality of words that are placed on the data lines in parallel.

11. An electronic data processing circuit according to Claim 9, wherein the bus controller (20) is arranged to select a sequence of a plurality of words that are placed on the data lines or a subset of the data lines in series.

12. A method of processing data, the method comprising

- supplying a plurality of data words with variable word size and addresses for those data words;
- placing data bits from the plurality of data words of less than the maximum word size on data lines of a bus (14) in a same bus cycle if more than one of the plurality of data words has a word size of less than the maximum word size;
- placing the addresses for respective ones of the plurality of data words on address lines of the bus (14) in a plurality of respective bus cycles.

13. A method of processing data, the method comprising

- supplying respective data words for output on data lines of a bus (14);
- selecting distribution of the data words over the data lines and/or over a temporal sequence in which the data words will be placed on the bus (14), taking account of a number of data lines whose logic level will change upon placing the words on the data lines, the distribution being selected to minimize the number of data lines that will change logic level among at least two possible distributions;
- placing the data words on the data lines of the bus (14) according to the selected distribution.